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(11) **EP 1 335 418 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention  
of the grant of the patent:  
07.09.2005 Bulletin 2005/36

(51) Int Cl.<sup>7</sup>: **H01L 21/027**, **H01L 21/28**,  
**H01L 29/423**

(21) Application number: **02001998.0**

(22) Date of filing: **05.02.2002**

(54) **Method of fabricating a T-shaped electrode**

Verfahren zur Herstellung einer T-förmigen Elektrode

Procédé de fabrication d'une électrode en forme de T

(84) Designated Contracting States:  
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU**  
**MC NL PT SE TR**

(43) Date of publication of application:  
13.08.2003 Bulletin 2003/33

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- **PATENT ABSTRACTS OF JAPAN** vol. 016, no. 486 (E-1276) 08 October 1992 & JP 04 177 738 A (MITSUBISHI ELECTRIC CORP) 24 June 1992
- **WHITE V. ET AL:** 'Use of photosensitive polyimide for deep x-ray lithography' **APPLIED PHYSICS LETTERS** vol. 66, no. 16, 17 April 1995, pages 2072 - 2073

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**EP 1 335 418 B1**

## Description

### BACKGROUND OF THE INVENTION

#### 1. Technical Field

[0001] The invention relates to a method of fabricating an electrode on a semiconductor substrate. In particular, the invention concerns fabrication of a vertically profiled electrode like a T-gate or a  $\Gamma$ -gate.

#### 2. Description of the Prior Art

[0002] The rapid progress in material growth and device fabrication has greatly improved the performance of semiconductor devices like heterostructure field effect transistors in recent years. Such semiconductor devices were conventionally provided with gate electrodes having a triangular cross section. However, scaling down of the profile geometry of triangular-shaped gate electrodes with the intention to achieve shorter electron transit times leads to a strong increase of the gate end-to-end resistance. This not only deteriorates the high-frequency performance of the semiconductor device but also its power-gain cutoff frequency and its noise behavior.

[0003] In order to solve the problems associated with triangular-shaped gate electrodes, vertically profiled gate electrodes like T- or  $\Gamma$ -shaped gate electrodes (T- or  $\Gamma$ -gates) have been proposed. Vertically profiled gate electrodes in the form of T- or  $\Gamma$ -gates combine small footprints, i.e., short gate lengths, with large cross-sectional areas.

[0004] Fabrication methods and fabrication limits of T- or  $\Gamma$ -gates are exemplarily discussed in B.E. Maile "Fabrication limits of nanometer T- and  $\Gamma$ -gates: Theory and Experiment", J. Vac. Sci. Technol. B 11(6), Nov/Dec 1993, pages 2502 to 2508. In this article fabrication of T- and  $\Gamma$ -gates in the sub-100 nm regime using electron beam lithography, multi-layer resist stacks and lift-off is described.

[0005] During fabrication of the T- and  $\Gamma$ -gates a bilayer resist stack is arranged on the semiconductor substrate. The bilayer resist stack is exposed by way of electron beam lithography and then developed in order to locally open and vertically as well as horizontally pattern the resist stack. After the resist stack has been patterned, a gate metal is deposited on the patterned resist stack and a lift-off is performed to remove the patterned resist stack together with the gate metal deposited thereon.

[0006] The bilayer resist stack consists of a first resist layer (bottom resist) arranged on the semiconductor substrate and a second resist layer (top resist) arranged on the bottom resist. Both resist layers are formed from positive electron resists. In a positive electron resist, electron-polymer interaction taking place during exposure by the impinging electrons causes chemical bonds

to be broken (chain scission) to form shorter molecular fragments. As a result, the molecular weight is reduced in the irradiated areas. The irradiated areas are later dissolved in a developer that attacks the low-molecular-weight material.

[0007] The T- and  $\Gamma$ -gate fabrication described above requires an electron dose profile as depicted in Fig. 1a. As can be seen from Fig. 1a, the electron dose profile consists of a quasi-line exposure 10 and an overlaid area exposure 12. The quasi-line exposure 10 defines the length of the gate in an x-direction and is also referred to as "core" exposure, whereas the overlaid area or "frame" exposure 12 defines the gate head. Changes of cross-sectional geometry, i.e., T- and  $\Gamma$ -shape, can easily be realized by changing the relative x-position of core and frame exposure.

[0008] As can be seen from Fig. 1a, the electron dose D1 required to expose the bottom resist is higher than the electron dose D2 for top resist exposure. This means that the sensitivity, which is defined as the electron dose required per unit area to give complete development, of the top resist is higher than the sensitivity of the bottom resist. Different resist sensitivities are necessary to control the vertical profiling of the gate electrode.

[0009] EP 0 718 877 A2 relates to a method of forming a vertically profiled mushroom-shaped gate electrode. During fabrication of the gate electrode, a photoresist structure is created that includes a patterned bottom layer made from a positive resist and a patterned top layer made from a negative resist. The top layer may be configured as a multi-layer.

[0010] US 4,373,018 relates to a top surface imaging technology for high-resolution patterning of a device surface. In a first step, a photoresist structure including an organic bottom resist layer and an inorganic top resist layer is created. Then, a pattern is produced in the inorganic layer by selective exposure and, after development of the inorganic layer, the pattern is replicated in the underlying organic layer by additional exposure.

[0011] Methods for forming vertically profiled electrodes using two layered resist patterns are known from each of EP 0 978 869 A2, US 5,370,973 and JP 04 177738. From these documents it is further known to utilize a bottom resist pattern that is made from a negative resist.

[0012] There is a need for a method of fabricating an improved semiconductor device having a vertically profiled electrode on a semiconductor substrate which allows a better control of the vertical electrode profile.

### SUMMARY OF THE INVENTION

[0013] According to the invention a method of fabricating a semiconductor device having a vertically profiled electrode on a semiconductor substrate is proposed, the method comprising the step of providing on the substrate a resist structure with at least a first negative resist pattern arranged on the substrate and hav-

ing a first opening and a second resist pattern having a second opening surrounding the first opening, the relative location of the first and the second opening defining a vertical profile of the electrode, and the further steps of depositing a metal on the resist structure, and of performing lift-off to remove the second resist pattern together with the metal deposited thereon. The first resist pattern is not or not totally removed during device fabrication.

**[0014]** Generally, the use of a negative resist as first resist has favorable implications for device fabrication and allows a better control of the vertical electrode profile. For example technological phenomena that conventionally, (i.e., when a positive resist is used as first resist) lead to an unwanted broadening of the gate length have the opposite effect when a negative resist is used. Thus a spreading of the dose or energy profile, an increase of the exposing beam diameter, of the exposure dose or, in the case of exposure by photons, of the exposure energy can be exploited to actually contribute to an effective reduction of the gate length and to faster semiconductor devices.

**[0015]** The second resist pattern may be arranged completely above the first resist pattern (resist stack) or adjacent to the first resist pattern directly on the substrate. Furthermore, the second resist pattern may be arranged partly above the first resist pattern and partly on the substrate.

**[0016]** The second opening in the second resist pattern is preferably larger than the first opening in the first resist pattern and may completely surround the first opening such that the resulting resist structure has a step-like profile in a vertical direction. In addition to the first and the second resist pattern the resist structure may comprise further resist patterns, preferably in the form of resist patterns arranged between the first and the second resist pattern or arranged for example with an overhang above the second resist pattern.

**[0017]** The resist structure may comprise electron resists or resists which are to be exposed by photons, like optical resists and X-ray resists. In the case the first resist is to be exposed by electron beam lithography, the first resist may comprise hydrogen silsesquioxane ( $\text{HSiO}_{3/2}$ )<sub>n</sub> (HSQ). Furthermore, the resist structure may comprise a combination of different resists. For example the first resist may be a resist to be exposed by electrons and the second resist may be a resist to be exposed by photons or vice versa. In such a case two or more different exposure methods are used. Whereas the first resist is a negative resist, the second resist may be either a positive or negative resist.

**[0018]** The first resist pattern may remain completely or partially on the substrate, i.e., is preferably not totally removed during device fabrication. In such a case the first resist pattern may function as a kind of passivation layer. According to an especially preferred embodiment, the first resist remains at least in cavities arranged between the substrate and portions of the vertically profiled

electrode.

**[0019]** The first resist may be a low-k dielectric, i.e., a dielectric having a low dielectric constant  $\epsilon_r$ . This is especially advantageous when the first resist pattern remains at least partially between an area of the substrate and the electrode because the low dielectric constant then leads to a reduction of device input and feedback capacities and improves device performance.

**[0020]** The first resist may be exposed using an inverted quasi-line energy or dose profile. A quasi-line is a line having limited extensions in two perpendicular directions, wherein the extension in one direction is much larger than the extension in the other direction. Such an energy or dose profile is especially advantageous if the electrode to be fabricated is a gate electrode. The exposed first resist may be developed using a selective developer. It can thus be ensured that the first resist can be developed separately from the second resist or any other resist used for electrode fabrication purposes. If necessary, the exposed second resist or any other exposed resist contributing the resist structure may also be developed using a selective developer.

**[0021]** The first and the second resist can be exposed either simultaneously or separately. If the first and the second resist are to be exposed simultaneously, the first resist may be arranged as a bottom resist on the substrate and the second resist may be arranged as a top resist on the first resist. On the other hand, if the first and the second resist are to be exposed separately, the first resist may be arranged on the substrate and developed prior to arranging the second resist on the first resist and/or on such areas of the substrate which have previously been opened by developing the first resist. The second resist may then be exposed separately from the first resist and developed in a subsequent development step.

**[0022]** The method discussed above allows fabrication of a semiconductor device comprising a substrate, a vertically profiled electrode arranged on the substrate, a cavity arranged between the substrate and the electrode, and a negative resist arranged in the cavity. The cavity may be constituted for example by a gap arranged between an upper surface of the substrate and the lower surface of the vertically profiled electrode facing the substrate.

**[0023]** The negative resist preferably fills the cavity at least to such an extent that the substrate remains covered in an area surrounding a contact area between the substrate and the electrode. More preferably, the negative resist is arranged such that the cavity remains hermetically sealed after deposition of the metal. Due to the comparatively high temperatures occurring during metal deposition the first resist may advantageously become hardened and tempered.

**[0024]** The negative resist, which may cover the substrate in an area outside the cavity or which may essentially be arranged only within the cavity, is preferably a dielectric having a dielectric constant  $\epsilon_r < 4.5$ . The area

of contact between the electrode and the substrate may be the bottom of an etched recess. This etched recess is preferably arranged under the negative resist.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0025]** Further aspects and advantages of the invention will become apparent upon reference to the following detailed description of preferred embodiments and the drawings, wherein

- Figs. 1a to 1d show the prior art dose profile and dose or energy profiles according to exemplary embodiments of the invention;
- Figs. 2a, 2b show a first embodiment of a method of fabricating a vertically profiled gate electrode on a semiconductor substrate according to the invention;
- Figs. 3 to 6 show four further embodiments of a method of fabricating a vertically profiled gate electrode on a semiconductor substrate according to the invention.

#### DESCRIPTION OF PREFERRED EMBODIMENTS

**[0026]** In the following, the invention is exemplarily set forth with respect to a plurality of embodiments relating to the fabrication of T- or  $\Gamma$ -shaped gate electrodes on semiconductor substrates. However, the invention is neither restricted to the specific electrode types nor to the specific profiles nor to the specific resist types discussed below. In particular, although the following discussion mainly relates to electron resists, the invention could also be practiced using additionally or solely resists which are to be exposed by photons (e.g. deep-UV, extreme UV, X-rays) or focused ion beams. Moreover, although the following discussion primarily relates to resist structures comprising two or three different resists and generally U-shaped dose or energy profiles, more complex resist structures and dose or energy profiles can be used also in order to fabricate more sophisticated vertical profiles. Furthermore, although in the following the combined use of a negative resist and one or more positive resists is described, the invention could also be practiced using solely negative resists or two or more negative resists in combination with one or more positive resists.

**[0027]** Typical dose or energy profiles according to the invention are exemplarily depicted in Figs. 1b to 1d. The term "dose profile" applies when the resists are exposed by electron or ion beams, and the term "energy profile" applies when the resists are exposed by photons. In the case the resist structure is fabricated using a mix of different exposure mechanisms, separate dose

and energy profiles would be involved. If for example fabrication of the resist structure comprises a resist exposed by electrons and a further resist exposed by photons, a mixed dose/energy profile could result.

**[0028]** The dose or energy profiles depicted in Figs. 1b to 1d could be the result of a single exposure step or could be the accumulation of a plurality of exposure steps. The profiles depart from the assumption that a combination of a negative resist as bottom resist and a positive resist as top resist is used to realize the resist structure defining the vertical gate profile. The negative resist is used for structuring the gate foot and the positive resist is used for structuring the gate head. As has been mentioned above, however, a negative resist could be used also for structuring the gate head.

**[0029]** The dose or energy profiles depicted in Figs. 1b to 1d deviate from the dose profile of Fig. 1a in that the exposure pattern of the "core" exposure 10 is inverted. In other words, the gate foot is defined by an inverted quasi-line exposure. In the cross section along the x-axis such an inverted quasi-line exposure has a local dose or energy minimum 14 at the position of the gate foot. The local minimum 14 is surrounded by two peaks 16 which lie above the critical energy  $E_1$  or the critical dose  $D_1$  required to expose the negative resist. The inverted quasi-line exposure defining the gate foot is combined with a frame exposure 12 which defines the shape of the gate head in the positive resist. The positive resist has a comparatively higher sensitivity ( $E_2/D_2$ ).

**[0030]** As a result of the inverted quasi-line exposure of the negative resist, any broadening of the peaks 16 due to an increase of an exposure dose or exposure energy or due to a broadening of the beam diameter leads to a narrowing of the local minimum 14. Such a narrowing results in a reduced gate length and faster devices. On the other hand, a broadening of the peak 10 of the prior art quasi-line exposure depicted in Fig. 1a results in an increased gate length and leads to a reduced device speed.

**[0031]** The two or more dose or energy profile peaks 16 may be flat as shown in Fig. 1b. They alternatively may have a more complex shape and may even be asymmetric in order to generate a tailored profile of the negative resist. This allows for an optimization of the shape of the gate electrode in the foot region, further enhancing device speed and lift-off yield. Two exemplary asymmetric peak profiles are depicted in Figs. 1c and 1d. As can be gathered from Figs. 1c and 1d, the asymmetric peaks 16 have a dose or energy profile that linearly (Fig. 1c) or stepwise (Fig. 1d) decreases towards the local minimum 14.

**[0032]** In the following several methods of fabricating T- and  $\Gamma$ -gates on a semiconductor substrate using total dose profiles similar to the dose profile depicted in Fig. 1b will exemplarily be described for electron resists.

**[0033]** Referring to Figs. 2a and 2b, fabrication of a recessed T-gate using two separate exposure steps will now be explained in more detail. In a first step depicted



in Fig. 2a, a substrate 20 is coated with a layer 22 of a negative resist. The negative resist layer 22 has a thickness between 40 nm and 300 nm, preferably between 80 nm and 150 nm. The negative resist arranged on the substrate 20 is an ordered three-dimensional polymer like hydrogen silsesquioxane (HSQ). HSQ is a negative electron-beam resist having a low dielectric constant. In B.E. Maile et al, Sub-10nm Linewidth and Overlay Performance Achieved with a Fine-Tuned EBP-5000 TFE Electron Beam Lithography System, Jpn. J. Appl. Phys. Vol. 39 (2000), pages 6836 to 6842, HSQ is mentioned as a test vehicle for electron beam system testing and benchmarking.

**[0034]** During a first electron beam exposure step 200 the negative resist arranged on the substrate 20 is exposed using an inverted quasi-line dose profile as depicted in Fig. 2a. The dose profile of Fig. 2a consists of two peaks 16 surrounding a local minimum 14. The electron beam used to expose the negative resist can be a gaussian beam or a shaped beam.

**[0035]** In the negative resist layer 22 the electron irradiation of step 200 causes irradiation-induced polymer cross linking. The cross linking creates a complex three dimensional structure with a higher molecular weight than said of the non-irradiated resist. The non-irradiated resist can thus be dissolved in step 202 using a developer like tetramethylammoniumhydroxide (TMAH) that does not attack the irradiated high-molecular-weight material.

**[0036]** During the first development step 202 the negative resist is removed in all areas that have not been irradiated in step 200.

**[0037]** Consequently, the negative resist pattern 24 remaining on the substrate 20 has locally the form of an inverted quasi-line pattern. Such an inverted quasi-line pattern comprises a central opening 26 in the form of a quasi-line, i.e., a line having limited extensions, the contours of which are defined by the negative resist pattern 24 remaining on the substrate 20. The opening 26 defines the form of the gate foot and in particular the gate length.

**[0038]** After the negative resist has been developed, the substrate 20 and the negative resist pattern 24 arranged thereon are coated with a positive resist in step 204 to form a positive resist layer 28 covering the substrate 20 and the negative resist pattern 24. The positive resist layer 28 may have a thickness between 200 nm and 2000 nm, preferably between 400 nm and 1000 nm. In the following it will be assumed that the positive resist is an electron resist like polymethylmethacrylate (PMMA) or another polymer which functions as positive resist. In principle, however, the following steps could also be performed if the positive resist was a resist to be developed by photons.

**[0039]** Referring now to Fig. 2b, the positive resist is exposed in step 206 using a frame exposure dose profile 12 as depicted in Fig. 2b. The frame exposure defines the shape and the position of the gate head. A superpo-

sition of the dose profile used during the first exposure step 200 (Fig. 2a) and the dose profile used in the second exposure step 206 (Fig. 2b) corresponds to the dose profile depicted in Fig. 1b.

**[0040]** After the positive resist has been exposed, a second development step 208 is performed to open the areas irradiated by electrons. For developing purposes, mixtures of methylisobutylketone (MIBK) and isopropanol (IPA) may be used.

**[0041]** During the second development step 208 the positive resist layer 28 is patterned such that an opening 30 is created. This opening 30 in the developed positive resist pattern 32 surrounds the opening 26 in the negative resist pattern 24. The negative resist pattern 24 and the positive resist pattern 32 together define a resist structure 34 having a symmetric, step-like vertical profile. As will become apparent from the discussion below, the contours and the relative location of the opening 26 in the negative resist pattern 24 and the opening 30 in the positive resist pattern 32 will define the vertical profile of the gate electrode.

**[0042]** It can be seen from Fig. 2b that the positive resist pattern 32 is arranged adjacent to the negative resist pattern 24 such that the substrate 20 is only accessible via the opening 26 in the negative resist pattern 24. In other words, there is no gap between the positive resist pattern 32 and the negative resist pattern 24. Furthermore, it should be noted that the negative resist pattern 24 could have been provided with a plurality of for example parallel quasi-line openings 26 and the opening 30 in the positive resist pattern 32 could have been arranged such that it surrounds this plurality of openings 26 in the negative resist pattern 24. Thus a gate structure having a single gate head and a plurality of gate feet can be fabricated.

**[0043]** After the positive resist layer 28 has been opened as depicted in Fig. 2b, recess etching is performed in step 210 to etch a recess 36 into the substrate 20 through the opening 30 in the positive resist pattern 32 and the opening 26 in the negative resist pattern 24. Recess etching may be performed for example wet-chemically or using a plasma.

**[0044]** After recess etching has been performed, a gate metal like Ti/Pt/Au or Al is deposited on the resist structure 34 and the substrate 20 in step 212. Gate metal deposition can be performed by evaporation, sputtering, etc.

**[0045]** During gate metal deposition most of the gate metal will be deposited as a layer 38 on the positive resist pattern 32. However, some gate metal will enter the opening 30 in the positive resist pattern 32 and will thus be deposited on the open surfaces of the negative resist pattern 24 and, through the opening 26 in the negative resist pattern 24, on the substrate 20. The gate metal deposited on the negative resist pattern 24 and the substrate 20 forms a gate electrode 40.

**[0046]** In a last step 214, lift-off is performed in an organic solvent like acetone or dimethylformamid (DMF).

During lift-off, the positive resist pattern 32 together with the gate metal layer 38 deposited thereon are removed. The structure remaining on the substrate 20 after lift-off comprises the gate 40 with its gate head 42 and its gate foot 44 as well as the negative resist pattern 24. This means that during device fabrication the negative resist pattern 24 is not removed but remains in an otherwise empty cavity between the upper surface of the substrate 20 and a lower surface of the gate head 42 facing the substrate 20.

**[0047]** The negative resist pattern 24 thus hermetically seals the gate electrode 40 and the recess 36. This not only improves device reliability but also facilitates further processing of the device. Moreover, since the negative resist which fills the cavity is HSQ, i.e., a negative resist having a low dielectric constant, device operation is improved due to reduced input and feedback capacities.

**[0048]** In the following four further embodiments of the invention will be described with reference to Figs. 3 to 6. Since the materials and processes used in the further embodiments are to a large extent identical with those discussed in conjunction with the embodiment depicted in Figs. 2a and 2b, an in-depth discussion of the processes and materials will be omitted. Instead, only the differences will be discussed in more detail. The embodiments depicted in Figs. 3 to 6 generally deviate from the embodiment depicted in Figs. 2a and 2b in that the positive resist and the negative resist are exposed simultaneously and in that the positive resist layer 28 is arranged on the negative resist layer 22 prior to exposure.

**[0049]** Referring now to Fig. 3, a resist stack comprising a negative resist layer 22 and a positive resist layer 28 is arranged on the substrate 20. The two resists are simultaneously exposed in step 300 using the dose profile depicted in Fig. 1b. After exposure a first development step 302 is performed to create the positive resist pattern 32 including the opening 30. Since in the embodiment of Fig. 3 the negative resist will be developed using a selective developer, the negative resist layer 22 is not yet opened during the first development step 302. Instead, a selective second development step 304 has to be performed to open the negative resist layer 22 and to create a negative resist pattern 24' including an opening 26. It should be noted that the non-irradiated areas of the negative resist layer 22 which are arranged under the positive resist pattern 32 are not removed during the second development step 304. The reason for this is the fact that the positive resist pattern 22 functions as mask and allows removal of the negative resist only through the opening 30 of the positive resist pattern 32.

**[0050]** In the embodiment depicted in Fig. 3 no recess etching is performed. The gate metal is thus deposited on the resist structure 34 in a step 306 following the second development step 304.

**[0051]** After gate metal deposition a lift-off is performed in step 308 as explained above in conjunction

with Fig. 2b. During lift-off only the positive resist pattern 32 together with the gate metal layer 38 deposited thereon is removed. The negative resist pattern 24' remains on the substrate 20 and essentially covers the whole substrate 20 except for a small area of contact ("foot print") between the gate electrode 40 and the substrate 20.

**[0052]** According to a first variant of the invention the negative resist pattern 24' remains as a protective layer on the substrate 20. According to a second variant of the invention a facultative third development step 310 is performed after lift-off to remove the remaining parts of the negative resist pattern 24' that have not been exposed during the exposure step 300 and that were masked by the positive resist pattern 32 during the second development step 304. The negative resist pattern 24 created during the third development step 310 corresponds to the negative resist pattern depicted in Fig. 2b (step 214). According to a third variant of the invention, the negative resist pattern 24', including the negative resist in the cavity between the gate head 42 and the substrate 20, is completely removed, for example by means of a plasma.

**[0053]** A method of fabricating a T-gate 40 on a semiconductor substrate 20 according to a third embodiment of the invention is depicted in Fig. 4. The embodiment depicted in Fig. 4 is based on the embodiment shown in Fig. 3 and comprises an additional recess etching step 406 prior to the deposition of the gate metalization in step 408.

**[0054]** A method of fabricating a T-gate 40 according to a fourth embodiment of the invention is shown in Fig. 5. According to the fourth embodiment, the semiconductor device 20 is fabricated using a trilayer resist stack comprising a HSQ negative resist bottom layer 22 arranged on the substrate 20, a positive resist mid layer 28 arranged on the bottom layer 22 and a positive resist top layer 50 arranged on the positive resist mid layer 28.

**[0055]** The top layer 50 has a thickness between 20 nm and 500 nm, preferably between 50 nm and 200 nm, and is formed from PMMA or another polymer that can act as a positive resist. The mid layer 28 has a thickness between 150 nm and 1500 nm, preferably between 300 nm and 900 nm, and is formed from poly(methylmetacrylate/methacrylic acid)-copolymer (P(MMA/MAA)) or another polymer or copolymer that can function as a positive resist.

**[0056]** The positive resist of the mid layer 28 is chosen such that it has a higher sensitivity than the positive resist of the top layer 50. This can be gathered from the (modified) dose profile depicted in Fig. 5. The combination of three different sensitivities allows to create a recessed resist structure and to thus improve the lift-off yields as will be discussed below.

**[0057]** After the trilayer resist stack depicted in Fig. 5 has been exposed in step 500 using the modified dose profile, a first development step 502 is performed in order to develop the top resist 50 and the mid resist 28

simultaneously (separate development steps could be used as well). Since the positive resist of the mid layer 28 has a higher sensitivity than the positive resist of the top layer 50, and due to the modified dose profile, the first development step 502 creates a top resist pattern 52 which has an overhang relative to the mid resist pattern 32. This overhang is due to the fact that an opening 54 created in the top resist layer 50 during the first development step 502 is smaller than an opening 30 created in the mid resist layer 28. In other words, the mid resist pattern 32 is recessed with respect to the top resist pattern 52.

**[0058]** During deposition of the gate metal in step 508 the overhanging top resist pattern 52 allows to control the lateral spacing 60 between the gate electrode 40 and the mid resist pattern 32. This controllable spacing 60 increases the lift-off yields because the organic solvent has an improved lateral access to the mid resist pattern 32. Furthermore, the overhang allows likewise to control the spacing between the gate electrode 40 and laterally neighboring electrodes, e.g. source and drain electrodes, not depicted in Fig. 5.

**[0059]** A method of fabricating a  $\Gamma$ -shaped gate electrode on a substrate 20 according to a fifth embodiment of the invention is depicted in Fig. 6. As can be gathered from the dose profile shown in Fig. 6, the two dose peaks 16, 16' surrounding the local dose minimum 14 have a different lateral dimension in x-direction. This means that unlike the T-gate electrodes discussed above in context with the previous embodiments, the gate foot 44 is no longer arranged in the middle of the gate head 42. As can be seen from Fig. 6, the gate foot 44 is shifted relative to the gate head 42 to the left. Apart from this difference the embodiment depicted in Fig. 6 corresponds to the embodiment discussed above in conjunction with Fig. 4.

## Claims

1. A method of fabricating a semiconductor device having a vertically profiled electrode (40) on a semiconductor substrate (20), the vertical electrode profile defining a cavity between the substrate (20) and the electrode (40), comprising:

a) providing a resist structure (34) on the substrate (20), the resist structure (34) containing at least

- a first resist pattern (24, 24') arranged on the substrate (20) and having a first opening (26), wherein the first resist pattern (24, 24') is made from a negative resist; and
- a second resist pattern (32) having a second opening (30) surrounding the first opening (26), the relative location of the first and the second opening (26, 30) de-

fining a vertical profile of the electrode (40);

b) depositing a metal (38) on the resist structure (34); and

c) performing lift-off to remove the second resist pattern (32) together with the metal (38) deposited thereon;

**characterized in that** the first resist pattern (24, 24') is not or not totally removed during device fabrication and remains at least partially on the substrate (20) in an area under the electrode (40).

2. The method of claim 1, wherein the first resist comprises hydrogen silsesquioxane or another electron resist.
3. The method of claim 1 or 2, wherein step a) comprises exposing the negative resist using an inverted quasi-line energy or dose profile.
4. The method of one of claims 1 to 3, wherein step a) comprises exposing the first and the second resist separately.
5. The method of one of claims 1 to 3, wherein step a) comprises exposing the first and the second resist simultaneously.
6. The method of one of claims 1 to 5, wherein the resist structure (34) contains a third resist pattern (52) arranged on the second resist pattern (32) and having an overhang relative to the second resist pattern (32).
7. The method of one of claims 1 to 6, further comprising the step of d) developing the first resist pattern (24').
8. The method of one of claims 1 to 7, wherein the second resist pattern (32) is made from a positive resist.
9. The method of one of claims 1 to 7, wherein the second resist pattern (32) is made from a negative resist.
10. The method of one of claims 1 to 9, wherein the first resist pattern (24, 24') remains on the substrate also in an area adjacent to the electrode (40).

## Patentansprüche

1. Verfahren zur Herstellung eines Halbleiterbauelements mit einer vertikal profilierten Elektrode (40) auf einem Halbleitersubstrat (20), wobei das vertikale Elektrodenprofil einen Hohlraum zwischen



dem Substrat (20) und der Elektrode (4) definiert, umfassend:

a) Vorsehen eines Lackgebildes (34) auf dem Substrat (20), wobei das Lackgebilde (34) zumindest enthält

- eine erste Lackstruktur (24, 24'), welche auf dem Substrat (20) angeordnet ist und eine erste Öffnung (26) besitzt, wobei die erste Lackstruktur (24, 24') aus einem Negativlack hergestellt ist, und
- eine zweite Lackstruktur (32), welche eine die erste Öffnung (26) umgebende zweite Öffnung (30) besitzt, wobei die relative Lage der ersten und der zweiten Öffnung (26, 30) ein vertikales Profil der Elektrode (40) definiert;

b) Abscheiden eines Metalls (38) auf dem Lackgebilde (34); und

c) Durchführen eines Lift-Off zum Entfernen der zweiten Lackstruktur (32) zusammen mit dem darauf abgeschiedenen Metall (38),

**dadurch gekennzeichnet, dass** die erste Lackstruktur (24, 24') während der Bauelementherstellung nicht oder nicht ganz entfernt wird und zumindest teilweise auf dem Substrat (20) in einem Bereich unter der Elektrode (40) verbleibt.

2. Verfahren nach Anspruch 1, wobei der erste Lack Wasserstoff-Silsesquioxan oder einen anderen Elektronenlack enthält.

3. Verfahren nach Anspruch 1 oder 2, wobei der Schritt a) das Belichten des Negativlacks unter Verwendung eines invertierten quasi-linienförmigen Energie- oder Dosisprofils umfasst.

4. Verfahren nach einem der Ansprüche 1 bis 3, wobei der Schritt a) das getrennte Belichten des ersten und des zweiten Lacks umfasst.

5. Verfahren nach einem der Ansprüche 1 bis 3, wobei der Schritt a) das gleichzeitige Belichten des ersten und des zweiten Lacks umfasst.

6. Verfahren nach einem der Ansprüche 1 bis 5, wobei das Lackgebilde (34) eine dritte Lackstruktur (52) enthält, die auf der zweiten Lackstruktur (32) angeordnet ist und einen Überhang bezüglich der zweiten Lackstruktur (32) hat.

7. Verfahren nach einem der Ansprüche 1 bis 6, weiter umfassend den Schritt des d) Entwickelns der ersten Lackstruktur (24').

8. Verfahren nach einem der Ansprüche 1 bis 7, wobei die zweite Lackstruktur (32) aus einem Positivlack hergestellt ist.

9. Verfahren nach einem der Ansprüche 1 bis 7, wobei die zweite Lackstruktur (32) aus einem Negativlack hergestellt ist.

10. Verfahren nach einem der Ansprüche 1 bis 9, wobei die erste Lackstruktur (24, 24') auch in einem sich an die Elektrode (40) anschließenden Bereich auf dem Substrat verbleibt.

## Revendications

1. Procédé de fabrication d'un dispositif à semi-conducteur ayant une électrode de profil vertical (40) sur un substrat semi-conducteur (20), le profil vertical de l'électrode définissant une cavité entre le substrat (20) et l'électrode (40), comprenant :

a) la fourniture d'une structure de résine (34) sur le substrat (20), la structure de résine (34) contenant au moins

- un premier motif de résine (24, 24') disposé sur le substrat (20) et ayant une première ouverture (26), dans lequel le premier motif de résine (24, 24') est fait d'une résine négative ; et
- un deuxième motif de résine (32) ayant une deuxième ouverture (30) entourant la première ouverture (26), la position relative de la première et de la deuxième ouvertures (26, 30) définissant un profil vertical de l'électrode (40) ;

b) le dépôt d'un métal (38) sur la structure de résine (34) ; et

c) le retrait pour enlever le deuxième motif de résine (32) ainsi que le métal (38) déposé sur celui-ci ;

**caractérisé en ce que** le premier motif de résine (24, 24') n'est pas ou n'est pas totalement retiré pendant la fabrication du dispositif et reste au moins partiellement sur le substrat (20) dans une région située sous l'électrode (40).

2. Procédé selon la revendication 1, dans lequel la première résine comprend du silsesquioxane d'hydrogène ou une autre résine électronique.

3. Procédé selon la revendication 1 ou 2, dans lequel l'étape a) comprend l'exposition de la résine négative en utilisant une énergie quasi-linéaire inversée ou un profil de dose.



4. Procédé selon l'une des revendications 1 à 3, dans lequel l'étape a) comprend l'exposition de la première et de la deuxième résines séparément.
  5. Procédé selon l'une des revendications 1 à 3, dans lequel l'étape a) comprend l'exposition de la première et de la deuxième résines simultanément. 5
  6. Procédé selon l'une des revendications 1 à 5, dans lequel la structure de la résine (34) contient un troisième motif de résine (32) disposé sur le deuxième motif de résine (32) et présentant un surplomb par rapport au deuxième motif de résine (32). 10
  7. Procédé selon l'une des revendications 1 à 6, comprenant en outre l'étape consistant à d) développer le premier motif de résine (24'). 15
  8. Procédé selon l'une des revendications 1 à 7, dans lequel le deuxième motif de résine (32) est fait d'une résine positive. 20
  9. Procédé selon l'une des revendications 1 à 7, dans lequel le deuxième motif de résine (32) est fait d'une résine négative. 25
  10. Procédé selon l'une des revendications 1 à 9, dans lequel le premier motif de résine (24, 24') reste sur le substrat même dans une région adjacente à l'électrode (40). 30
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- 50
- 55

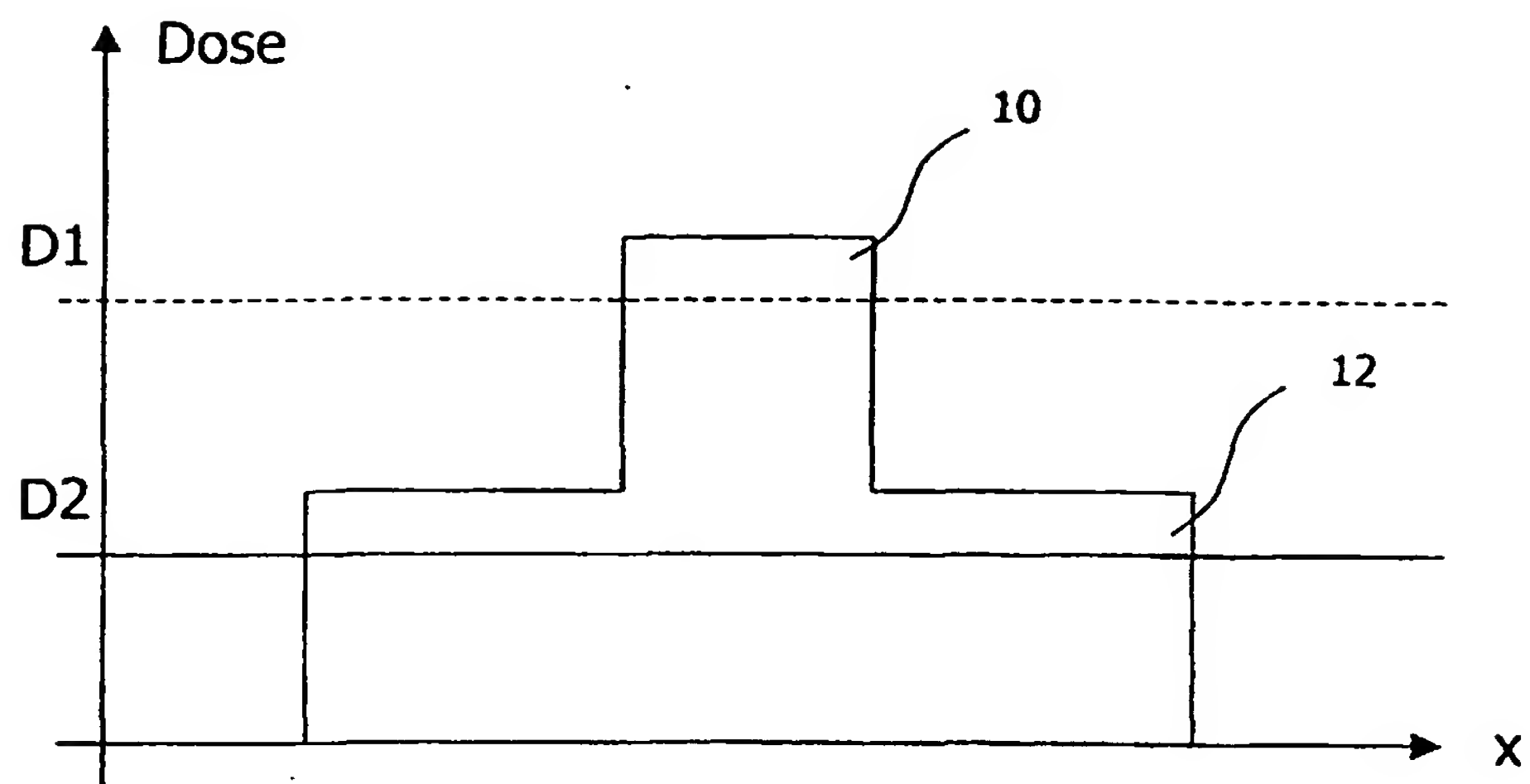


Fig. 1a Prior Art

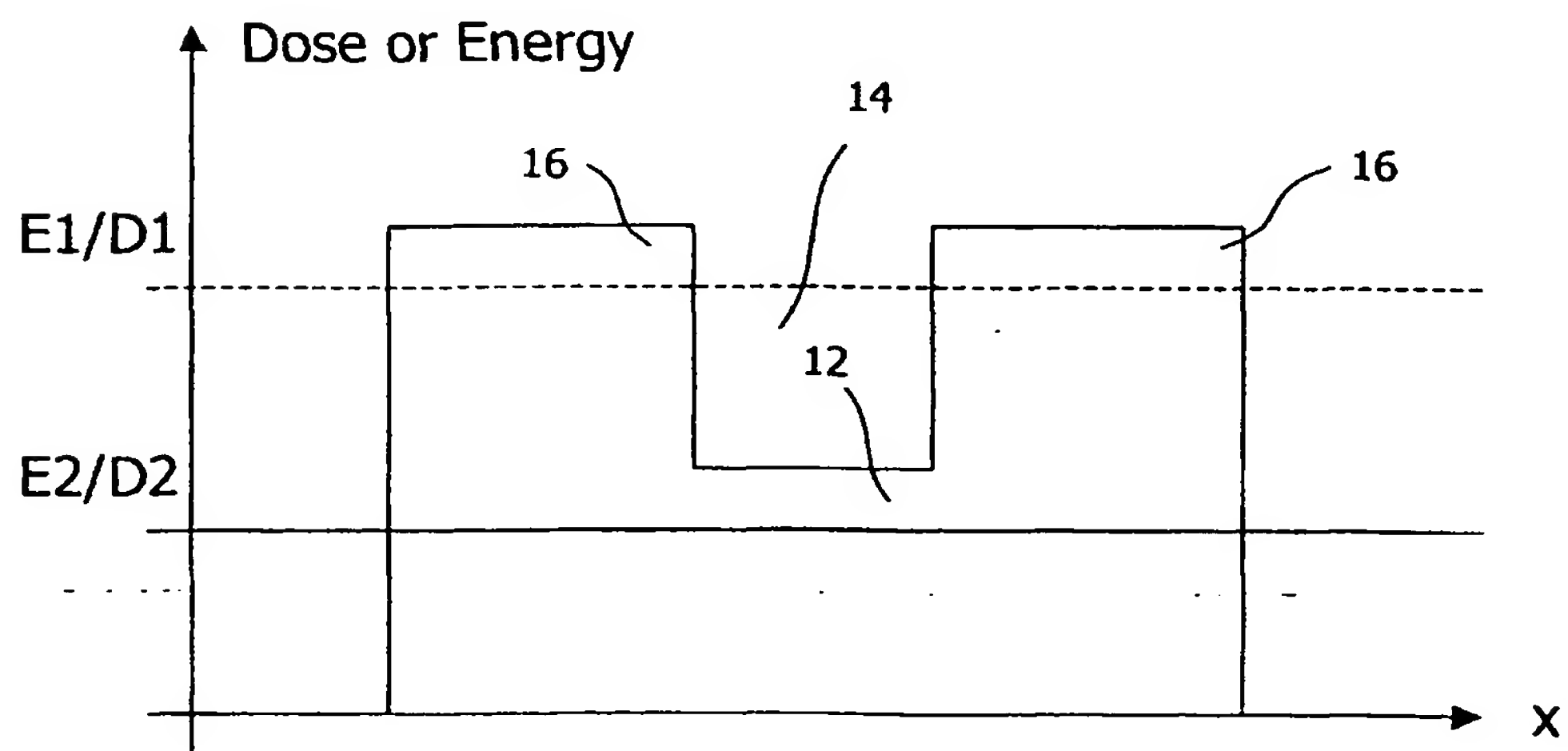


Fig. 1b

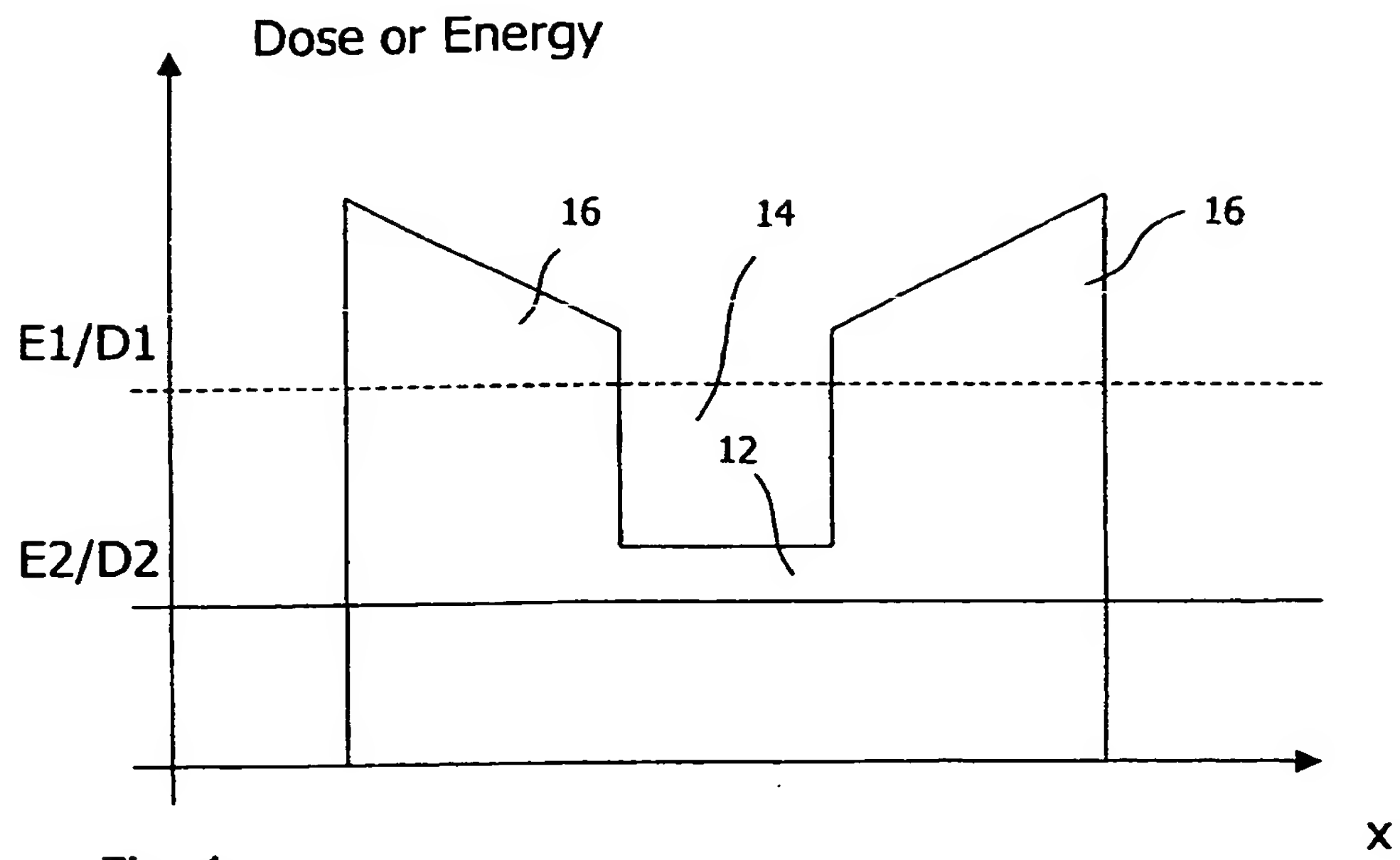


Fig. 1c

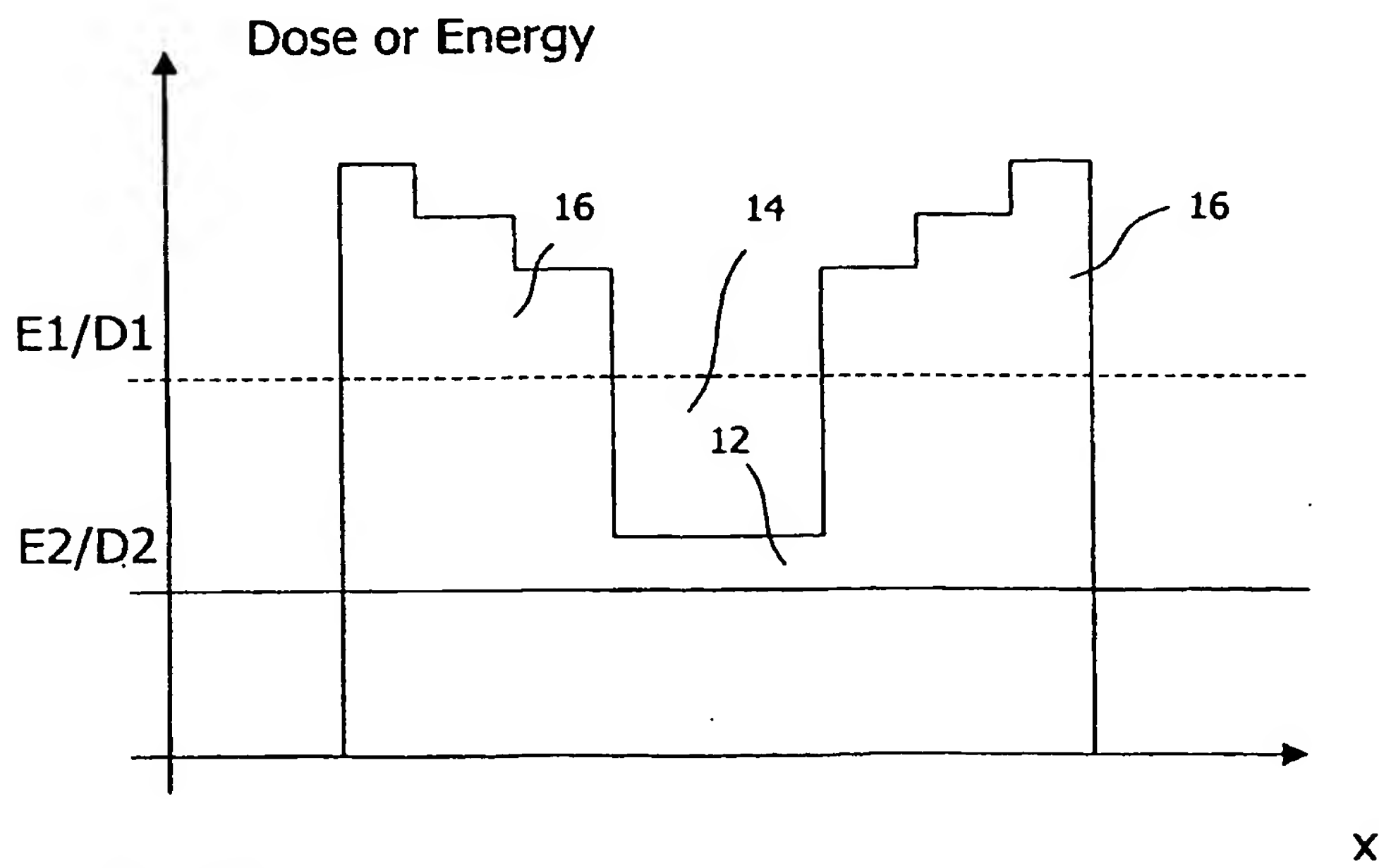


Fig. 1d

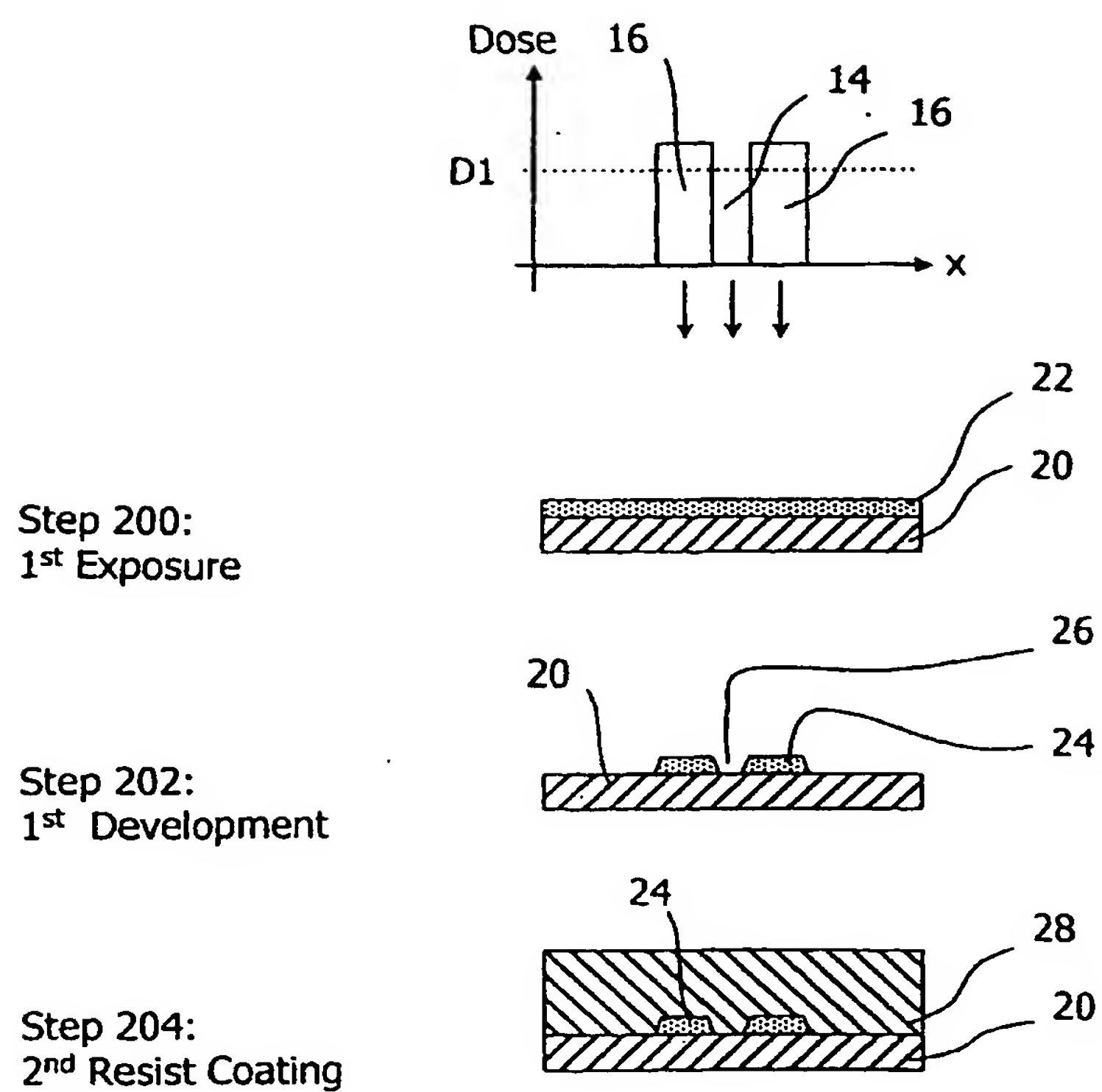


Fig. 2a



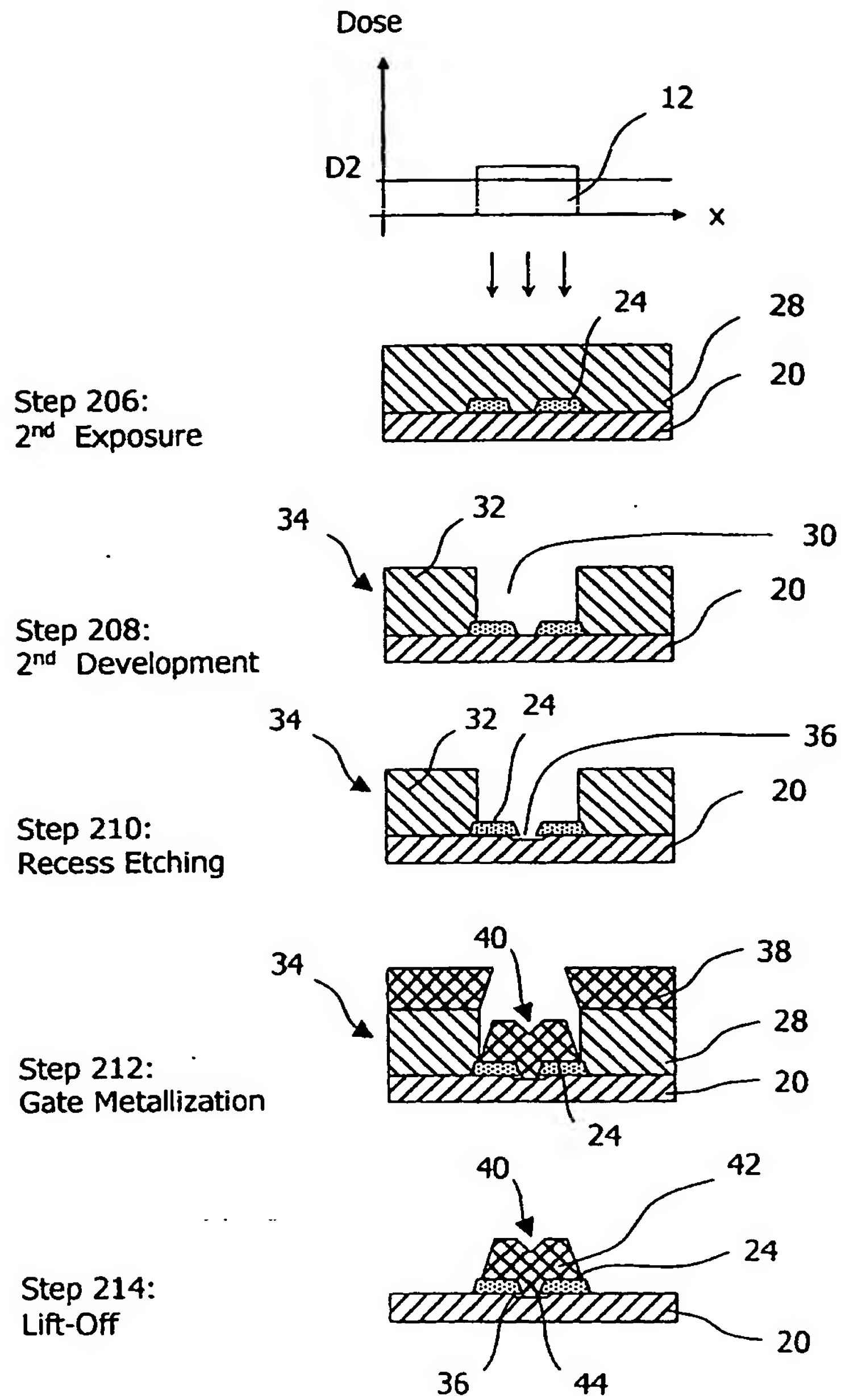


Fig. 2b

Fig. 3

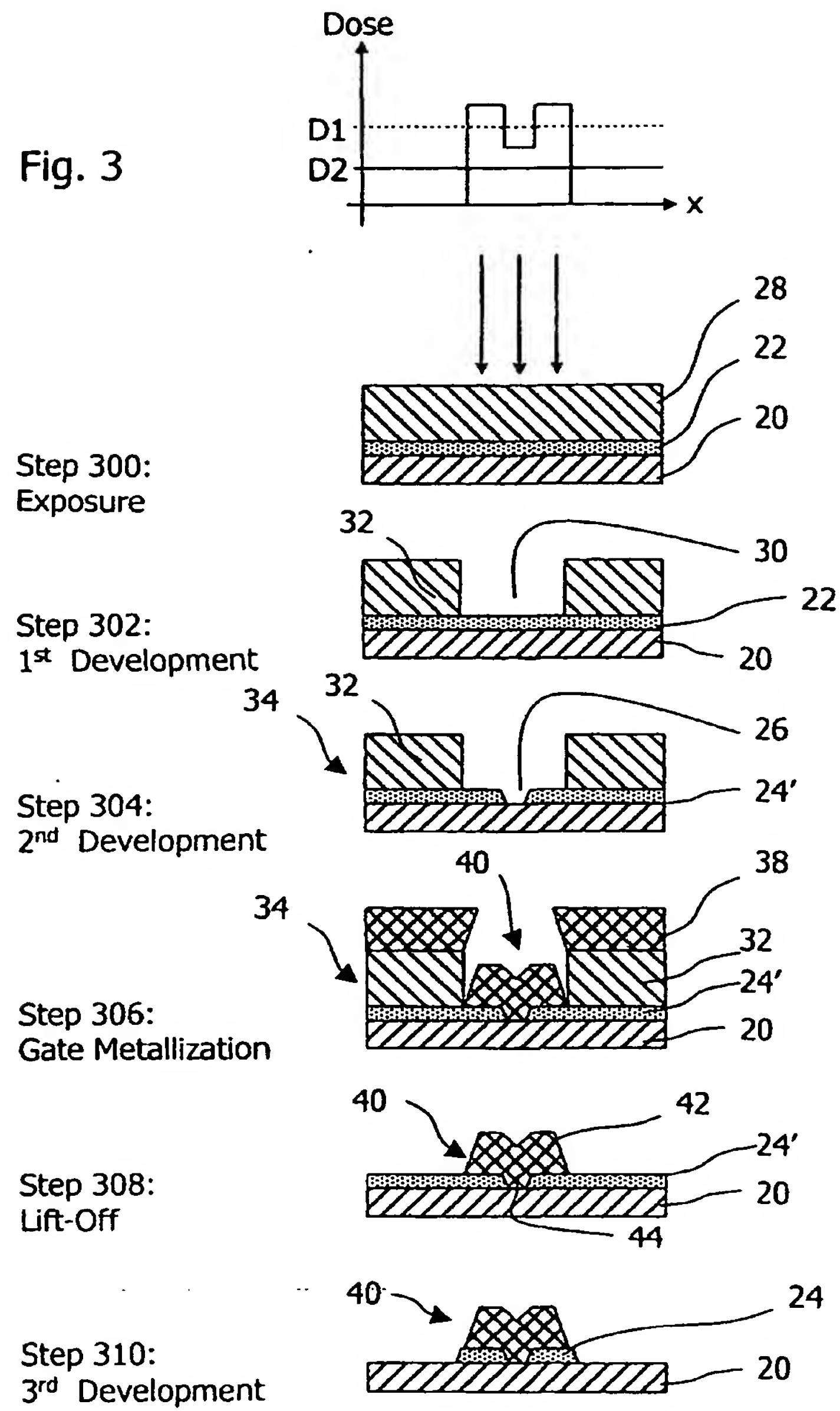


Fig. 4

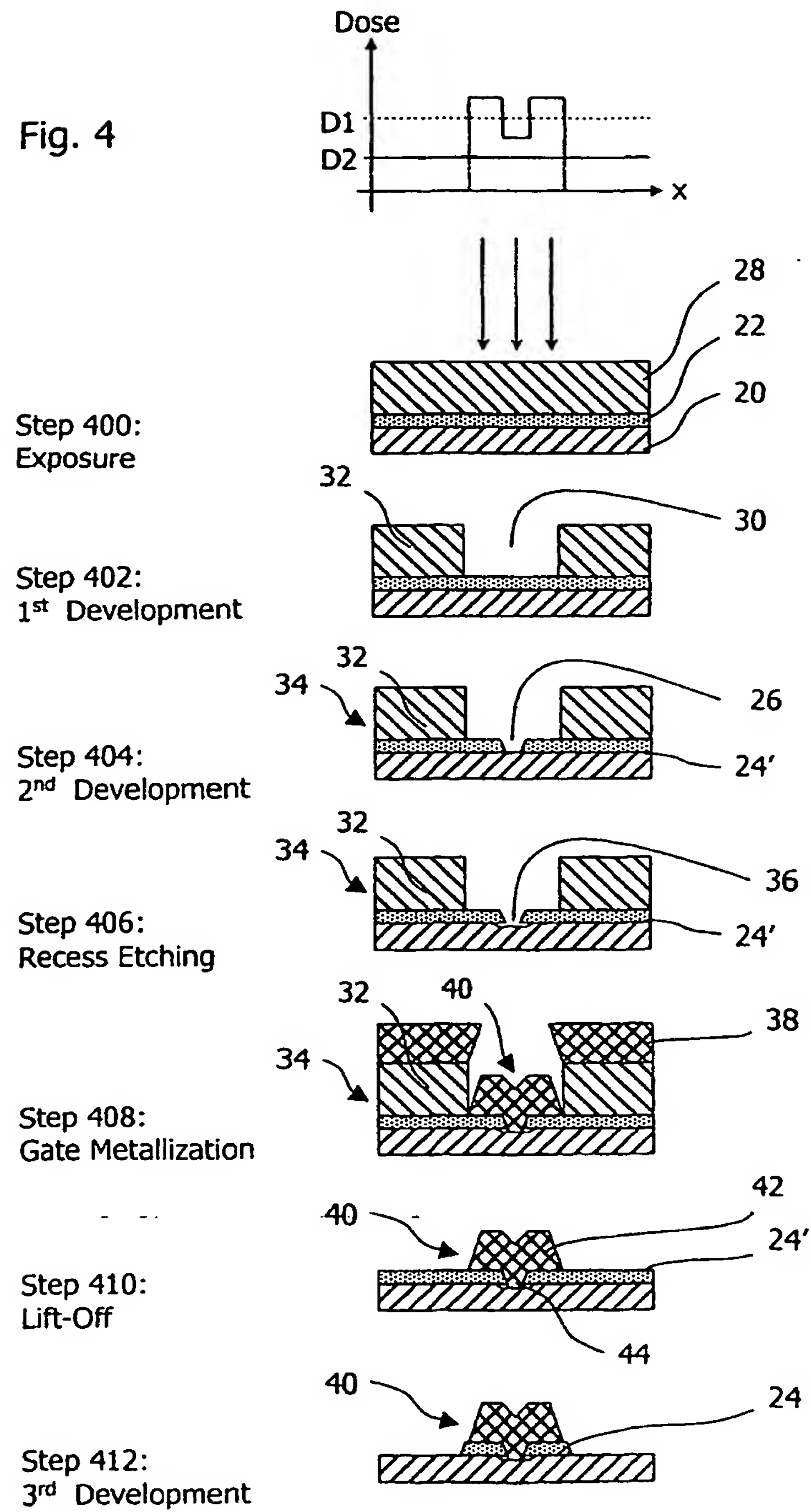


Fig. 5

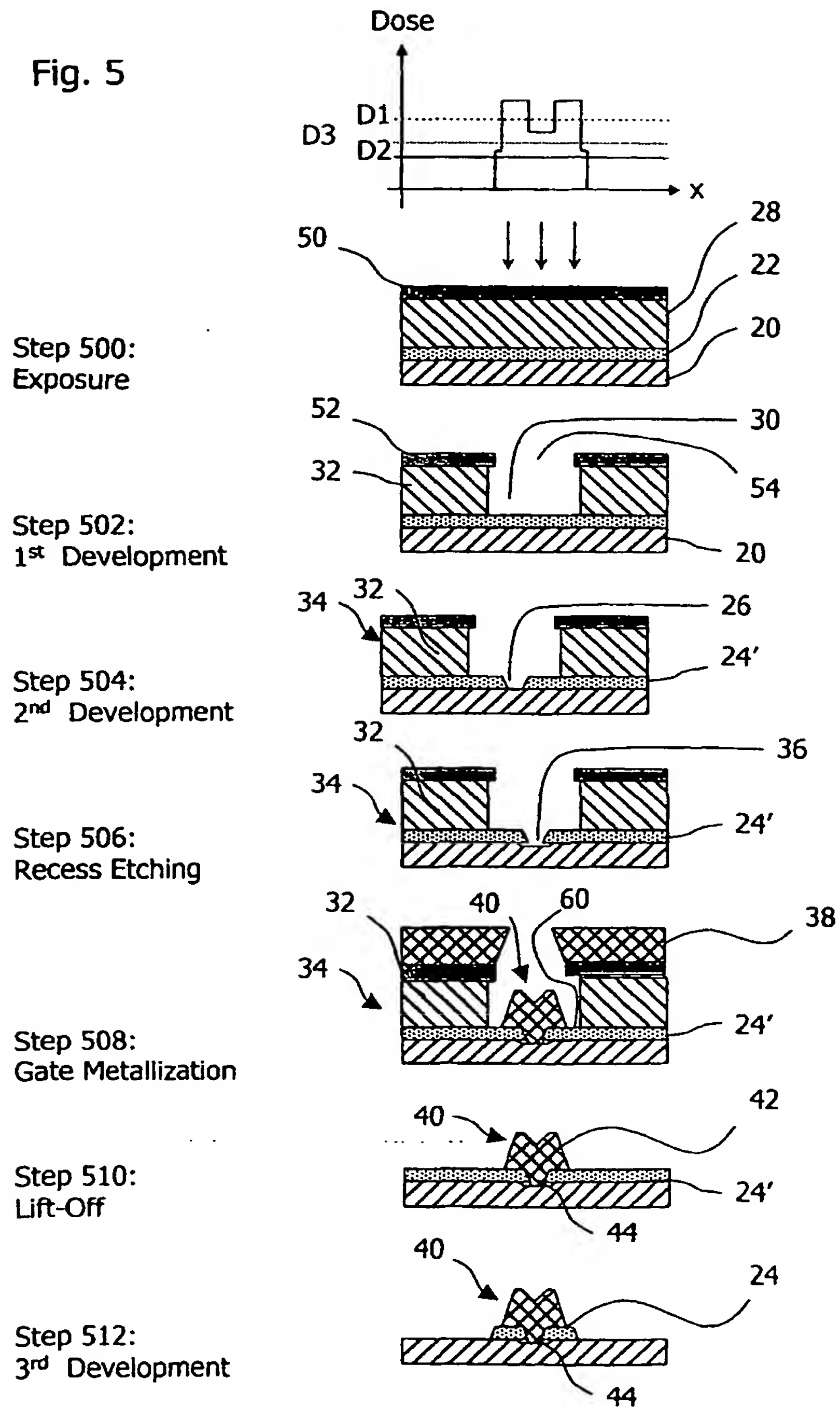
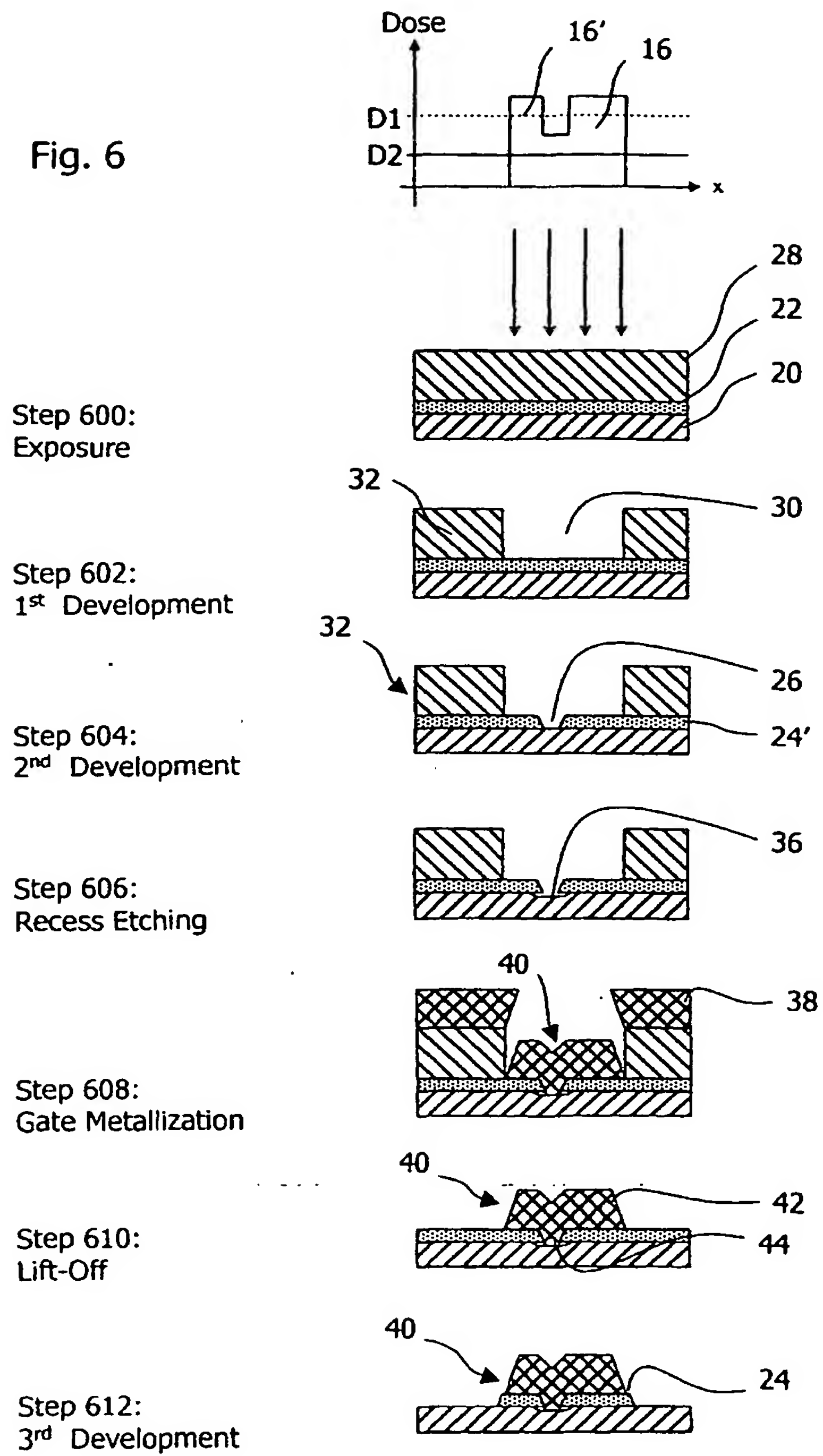




Fig. 6



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